REMARKS

Applicant respectfully traverses and requests reconsideration.

Furthermore, Applicant also wishes to thank the Examiner for notice that claims 1, 6, 12 and 17 have been allowed.

Applicant's attorney wishes to thank the Examiner for the courtesies extended during the telephone conference of February 10, 2004. As discussed with respect to claim 7, Applicant's attorney attempted to point out that the Nakatsuka reference appears to merely teach a single level of translation whether it be from the perspective of the graphics processor or from the data processor. The Examiner indicated that element (d) of claim 7 was taught in column 9, lines 40-55 where it states that "in this case, it is sometimes necessary to provide an address converter unit for converting a picture logical address into a physical address in order to effect access to the matrix data by the graphics processor 120." Applicant's attorney pointed out that this teaches only a single translation and also noted that the use of the term "picture logical address" in the Nakatsuka reference is equivalent to the term "logical address" with reference to the graphics processor as is specifically stated in column 8, lines 52-54 where it states "the logical address of the graphics processor or picture logical address has the tile type arrangement shown in FIG. 3C." As such, the cited portion of the reference appears to only teach a single translation by the graphics processor even in the alternative embodiment starting in line 40, column 9 wherein a picture logical address is translated into a physical address. Applicant is hopeful that after further consideration of the Nakatsuka reference in view of the Applicant's remarks, the claims will be passed to allowance.

In addition, the Nakatsuka reference specifically teaches that no address translation occurs for example by allowing the physical address and the picture physical address to directly

correspond to the pixel data. This is stated for example in column 8, lines 66 through column 9, line 3 where it states:

> By allowing the physical address and the picture physical address to directly correspond to the pixel data to speed up the picture processing, it becomes possible to effect access between the pixel region of the memory unit 200 and the graphics processor 120 without address translation (emphasis added)...

As such, the Nakatsuka reference teaches embodiments where the physical address and the picture physical address are the same address and hence no translation is required, or alternatively only where a single level translation occurs. There does not appear to be any teaching or suggestion of a second translation of an already translated address in the manner set forth in claims 7 and 18 as again clarified further below.

Claims 1 and 12 have been amended to correct typographical errors resulting from the amendment of said claims in a previous Amendment and Response mailed on January 29, 2003. Specifically, with respect to claim 1, the fourth limitation, "caching the physical address in a translation look aside table," should be moved within claim 1 such that reads before the eighth limitation, "when the physical page address corresponds to a physical address that requires further translation, retrieving a second physical page address." As stated in the previous Response mailed January 29, 2003, Applicant amended claim 1 "to include the respective limitations corresponding" to its depend claims. The phrase "caching the physical address in a translation look aside table" corresponded to originally filed claim 3 which was dependent upon originally filed claim 2. To maintain consistency with the originally filed claims and the presently amended claim 1, Applicant respectfully requests the aforementioned amendment. With respect with claim 12, Applicant respectfully maintains that the Amendment and Response

mailed January 29, 2003 also indicated the Applicant's desire to incorporate originally filed claim 14 within claim 12. As such, Applicant respectfully requests the phrase "caching the physical address in a translation look aside table" to be moved such that it reads before the limitation stating "retrieve a second physical page address when the physical page address corresponds to a physical address that requires further translation."

Claims 7 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakatsuka et al., U.S. Patent No. 6,433,782 ("Nakatsuka") and Bogin et al., U.S. Patent No. 6,192,455 ("Bogin"). Applicant respectfully repeats the relevant remarks made from the previous Amendment and Response mailed October 14, 2003. Specifically, Applicant respectfully maintains that no combination of Nakatsuka or Bogin teaches or suggests Applicant's claims 7 and 18.

As previously stated, Nakatsuka, among other differences, fails to teach a *multiple translation process* as claimed by Applicant. Applicant respectfully maintains that Nakatsuka remains silent as to any process or method comprising the steps of, *inter alia*, "a) translating a virtual address into an address; b) determining whether the address corresponds to translation memory space; . . . and . . . d) translating the address into another address when the address corresponds to translation memory space." (claim 7).

The Office Action appears to cite Column 9, lines 40-50, of Nakatsuka as teaching Applicant's multiple translation process as claimed in claim 7. However, Applicant respectfully notes that in addition to the Office Action having never cited this particular reference within Nakatsuka, the cited passage does not disclose a second translation of an address into another address as required by Applicant's claim 7. Instead, Applicant respectfully notes that the passage appears to teach an alternate embodiment of the process disclosed by Nakatsuka. In

particular, Applicant notes that the first embodiment of the Nakatsuka reference corresponds to: (1) the graphic processor accessing pixel data of memory without address translation because the physical addresses and picture logical address of the graphic processor correspond to one another (Col. 8, line 66-Col. 9, line 5); and (2) the data processor accessing pixel data by converting a logical address of the data processor into the picture logical address or physical address (Col. 9, lines 5-8). Nakatsuka discloses that the process in which the data processor accesses pixel is performed vis-à-vis a conventional translation approach. (Col. 9, lines 9-12).

As stated in the previous Amendment and Response mailed October 14, 2003, Applicant respectfully notes that Nakatsuka merely discloses a single translation. In Nakatsuka's first embodiment, a translation may only occur when the data processor accesses memory. When the data processor accesses the graphics region of memory, the address is converted into a physical address corresponding to the graphics region (i.e., the picture logical address). (Col. 9, lines 5-8; lines 13-20). However, when the data processor accesses the program region of memory, the address is converted into the physical address corresponding to the program region (Col. 9, lines 20-22). As stated *infra*, access by the graphics processor to the pixel data of memory (i.e., either segment of memory) requires no address translation (Col. 8, line 66 – Col. 9, line 5) because the arrangement of the pixel data assigned to both the program and data region is the same as that assigned by the picture logical address of the graphics processor (Col. 8, lines 52-57; Fig. 3D).

In a second embodiment, corresponding to the Office Action's citation to Col. 9, Nakatsuka discloses that when the data processor calculates a matrix (assumedly, a form of program data), the matrix data can be stored in the memory unit as a physical address in the form of a tile-type address. (Col. 9, lines 40-47). The reference continues to teach that in this second embodiment, it is sometimes necessary to provide an address converter unit for converting a

pixel logical address (i.e., the address scheme of the graphics processor) into a physical address in order to effect access to the matrix data by the graphic processor. (Col. 9, lines 47-50). It appears that this citation teaches that in a unique and separate second embodiment only a single address translation may occur between the graphics processor and a matrix stored in memory vis-à-vis an address converter unit. Nakatsuka's second embodiment does not teach or suggest a second address translation of a previously translated address.

Contrary to the Office Action, Applicant respectfully notes that two translations are not required to allow the graphic processor to access data. Instead, the additional Nakatsuka reference merely discloses an alternate embodiment of the reference where, again, only a single translation is utilized to allow a particular processing unit (i.e., the data or graphic processor) within the data processing apparatus to access a particular section of a memory (i.e., the program or graphic region).

Moreover, Applicant respectfully maintains that Nakatsuka fails to disclose Applicant's step (b) wherein, after a virtual address is translated into an address, a determination is made as to whether the address corresponds to translation memory space. The Office Action appears to cite Column 9, lines 13-22 as teaching or suggesting the claimed limitation. However, the particular reference to Column 9 merely discloses the method in which a data processing apparatus determines which region of memory the data processor is trying to access while operating in a first embodiment of Nakatsuka. That is to say, the cited reference is merely an explanation as to how the data processor determines whether or not the data it is accessing belongs to the program region or graphic region of memory. Applicant respectfully notes that step (b) of claim 7 impacts the claimed method for virtual address translation by determining whether or not the translated address (resulting from the method of step (a)) must be translated

into another address (as performed by step (d)). Because Column 9, lines 13-22 of Nakatsuka impacts only the original and sole translation of the virtual address into an address as performed by a data processor accessing memory, the cited reference does not render obvious or affect a second address translation in a manner analogous to Applicant's step (b) of claim 7.

As a result of the foregoing arguments, Applicant respectfully maintains that Nakatsuka fails to disclose a multi-step translation process wherein a virtual address is first translated into an address (see step (a)), and then, wherein, the translated address is then translated into another address when the address corresponds to translation memory space (see step (d)).

With respect to Bogin, Applicant respectfully repeats the relevant remarks made in the Amendment and Response mailed January 29, 2003. Specifically, Applicant notes that Bogin discloses a method and apparatus for preventing access to a system management random access memory space utilizing a *single* virtual to main memory address translation step. In no event does Bogin disclose a multiple translation process as claimed by Applicant. Moreover, while Bogin teaches that a single translated address is stored in a translation look aside table (i.e., the GTLB) when the translated address does not correspond to protected SMRAM memory space, the reference is silent as to Applicant's claimed invention wherein two translated addresses are stored in a single translation look aside table. As a result of the foregoing argument, Applicant respectfully maintains that Bogin fails to disclose a multistep translation process wherein a virtual address is first translated into an address and then, wherein the translated address is then translated into another address when the address corresponds to translation memory space.

Similar to Nakatsuka, Bogin discloses two embodiments. The first embodiment corresponds to the situation in which a non-AGP request is forwarded to an arbiter. In this event, no translation is needed. The second embodiment corresponds to the situation in which an AGP

request is forwarded to an arbiter. In this alternate event, a translation is required and the arbiter forwards the request to an AGP translator for address translation. (Fig. 3, elements 320, 310, 311, 308). The AGP translator looks first to the GTLB in the host bridge to determine whether or not there is a corresponding main memory address stored. In the event that a corresponding main memory address is found in the GTLB, then the AGP translator translates the address of the request to the corresponding main memory address. (Col. 5, lines 9-15; Fig. 3, element 328). However, in the event that a corresponding address is not found within the GTLB, then the AGP translator determines a corresponding translation table address for the request. (Col. 5, lines 18-21; Fig. 3, element 326). Upon determining a corresponding translation table address for the request, a cycle tracker (Fig. 3, element 312) forwards the request to a memory interface which fetches the corresponding main memory address from the translation table and forwards it back to the AGP translator (Col. 5, lines 43-55; Fig. 3, elements 327, 306, 315, 308). Upon receiving the translated address, the AGP translator determines whether or not the translated address falls within protected SMRAM address range. If the translator address is not within the SMRAM address range, then the GTLB is updated with a new translation entry. Otherwise, the translator address is converted into a non-SMRAM address such that the request does not access a protected region within memory (Col. 5, lines 55-63).

In summary, Bogin discloses a method and apparatus in which only a *single* translation may occur and wherein only a single translated addressed is stored in a graphics translation lookaside buffer. Because Bogin only suggests one address translation, it does not appear that Bogin is capable of also disclosing a method wherein both a translated address and a further translated address are cached in the same translation look aside table.

Because neither Bogin nor Nakatsuka teach or disclose, individually or in combination, Applicant's claim 7, Applicant respectfully believes that claim 7 is in proper condition for allowance. No combination of either reference discloses Applicant's multiple address translation method. Similarly, no combination of either reference renders obvious Applicant's step (b) wherein a determination is made, *after* a virtual address is translated into an address, whether the address corresponds to translation memory space. Moreover, no combination of references suggests caching *both* translated addresses in the same translation look aside table.

Because claim 18 corresponds to the module claim of Applicant's claim 7, claim 18 is also believed to be allowable for the same reasons as claim 7.

Claims 8-11 and 19-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nakatsuka et al. and Bogin et al. and further in view of Hayes et al., U.S. Patent No. 6,356,989. Applicant respectfully notes that claims 8-11 and 19-22 are dependent claims of allowable parent claims 7 and 18, respectively. As such, Applicant reasserts the relevant remarks made above with respect to allowable claims 7 and 18. Furthermore, Applicant submits that claims 8-11 and 19-22 are allowable as written for the same or similar reasons. Applicant further submits that the depending claims are also allowable in light of the presence of novel and non-obvious elements contained therein that are not otherwise present in the parent claim.

Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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